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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/757,764	01/09/2001	Daniel J. Scales	9772-0268-999	8427

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Pennie & Edmonds, LLP
3300 Hillview Avenue
Palo Alto, CA 94304

EXAMINER

YIGDALL, MICHAEL J

ART UNIT	PAPER NUMBER
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2122

DATE MAILED: 12/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/757,764

Applicant(s)

SCALES, DANIEL J.

Examiner

Michael J. Yigdal

Art Unit

2122

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 January 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 January 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-36 are pending and have been examined. The priority date considered for the application is 9 January 2001.

Specification

2. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are: In the detailed description of Fig. 3 on page 10, under the heading "The Static Single Assignment Graph," item 342 is referred to as a value, as a plurality of values, and as a plurality of nodes; furthermore, although items 342 and 344 are recited in the specification, Fig. 3 shows several items labeled 342-1, 344-1, 342-2, 344-2, and so on.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 2, 5, 7-14, 17, 19-26, 29, and 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,758,051 to Moreno et al. (hereinafter Moreno) in view of U.S. Pat. No. 5,787,287 to Bharadwaj.

With respect to claim 1, Moreno discloses a method for modifying serial dependencies in a procedure (see column 9, lines 38-45).

Moreno does not expressly disclose the steps of:

(a) building a graph representation of said procedure, said graph representation having an origin and including a unique position, relative to said origin, for each memory operation in said procedure;

(b) designating a location type for each memory operation in said graph representation; each said location type based on a characteristic of said corresponding memory operation;

(c) identifying a first memory operation having the same location type as a second memory operation; wherein said first memory operation is positioned closer to said origin than said second memory operation, and said graph representation does not include any additional memory operations of the same location type between the first and second memory operations;

(d) determining whether said graph representation includes at least one program operation between said first and second memory operations, and when said determination is positive, moving said second memory operation to a new position in said graph representation that is closer to said first memory operation.

Moreno does show reordering memory operations and scheduling the related instructions (see Fig. 2A). Moreno also shows moving a second memory operation to an earlier position, closer to a first memory operation, as in step (d) above (see column 9, lines 55-67).

Bharadwaj discloses step (a) above in terms of building vectors to represent data dependency and control flow paths for instructions in a procedure (see Fig. 3 and column 3, lines

32-35; see also Fig. 2 and column 3, lines 50-56, which shows a control flow diagram or graph having an origin and a unique position for each memory operation).

Bharadwaj further discloses step (b) above in terms of designating each memory operation according to its associated variable, i.e. its data type, and classifying each instruction as a reader or a writer based on its characteristics (see column 4, lines 4-25).

Bharadwaj further discloses steps (c) and (d) above in terms of computing the dependency path vectors between two instructions (see column 5, lines 3-5, which shows identifying two memory operations that operate on the same variable, i.e. that have the same location type; see also column 4, lines 52-58, which shows that one memory operation comes before the other, i.e. is closer to the origin; see also column 5, lines 5-10, which shows that no related instructions are included between the two memory operations; see also column 5, lines 10-15, which shows determining that there is another operation between the two memory operations; see also column 7, lines 10-12, which shows scheduling or moving code).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Moreno with the features taught by Bharadwaj, for the purpose of determining whether reordering memory operations affects the meaning of the source code (see Bharadwaj, column 6, lines 40-43).

With respect to claim 2, Moreno does not expressly disclose the limitations wherein:

(a) the building step includes the step of assigning an initial set of serial dependencies between program operations represented in said graph representation;

(b) the moving step includes (i) removing one or more of the serial dependencies in said initial set of serial dependencies that is associated with said second memory operation and (ii)

Art Unit: 2122

creating a new serial dependency between said first memory operation and said second memory operation.

Moreno does show moving memory operations in the schedule of instructions, thereby modifying serial dependencies (see column 9, lines 38-45).

Bharadwaj further discloses limitation (a) above in terms of computing an initial set of dependency path vectors between instructions (see column 6, lines 51-54).

Bharadwaj further discloses limitation (b) above in terms of moving code, which removes serial dependencies, and computing a new set of dependency path vectors (see column 6, lines 55-66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Moreno with the features taught by Bharadwaj, for the purpose of determining whether reordering memory operations affects the meaning of the source code (see Bharadwaj, column 6, lines 40-43).

With respect to claim 5, Moreno further discloses the limitation wherein said moving step results in said second memory operation being advanced in a schedule of machine instructions (see column 9, lines 55-67, which shows moving a second memory operation to an earlier position, i.e. advancing the operation in the schedule of instructions).

With respect to claim 7, Moreno further discloses the limitation wherein said first memory operation is a store or an array store and said second memory operation is a load or an array load (see column 9, lines 63-67, which shows the case wherein the second memory operation is a load and the first memory operation is a store).

Art Unit: 2122

With respect to claim 8, Moreno further discloses the limitation wherein said procedure includes a calling procedure and said first memory operation is in said calling procedure and said second memory operation is in a called procedure that is called by an operation in said calling procedure (see column 9, lines 33-48, which shows scheduling all the instructions in a program, including those associated with a procedure called by another procedure; note that a calling procedure may include a first memory operation and a called procedure may include a second memory operation).

With respect to claim 9, Moreno further discloses the limitation wherein said moving step results in a placement of said second memory operation in said calling procedure (see column 9, lines 33-48, which shows moving a second memory operation to an earlier position in the schedule of instructions; note that this applies to all the instructions in a program, and could result in moving a second memory operation from a called procedure to a calling procedure).

With respect to claim 10, Moreno does not expressly disclose the limitation wherein said location type of each memory operation is selected from the group consisting of a predefined set of base types, a predefined set of array types, object types, and object field types.

Bharadwaj further discloses the limitation above in terms of identifying memory operations that reference a particular variable, i.e. memory operations associated with the same data type (see column 4, lines 4-15; note that the data type or location type of a variable is necessarily selected from a predefined set of base types and array types, or from a set of object types and object field types defined in the code).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Moreno with the features taught by Bharadwaj, for the

purpose of determining whether reordering memory operations affects the meaning of the source code (see Bharadwaj, column 6, lines 40-43).

With respect to claim 11, Moreno does not expressly disclose the limitation wherein the building step further comprises adding a global store dependency to each operation in said procedure that reads a variable from or stores a variable to memory.

Bharadwaj discloses the limitation above in terms of computing dependency path vectors for each instruction that reads or writes a variable (see column 4, lines 4-15; note that a store dependency would be added to each operation following a store instruction that references the same variable).

Moreno further discloses the step of generating a schedule of machine instructions in accordance with said graph representation, wherein each said machine instruction in said schedule of machine instructions, which corresponds to an operation that reads a variable from or stores a variable to memory, is ordered in accordance with said global store dependency associated with said operation (see Fig. 1, which shows generating a schedule of instructions; see also column 9, lines 59-67, which shows verifying that memory operations are ordered in accordance with a store dependency).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Moreno with the features taught by Bharadwaj, for the purpose of determining whether reordering memory operations affects the meaning of the source code (see Bharadwaj, column 6, lines 40-43).

With respect to claim 12, Moreno does not expressly disclose the limitation wherein a first operation affects a value of a variable stored in memory and a second operation serially

follows said first operation, said building step further comprising adding a global store dependency from said second operation to said first operation.

Bharadwaj discloses the limitation above in terms of computing dependency path vectors for each instruction that reads or writes a variable (see column 4, lines 4-15; note that a store dependency would be added from a second operation to a first operation when both instructions reference the same variable).

Moreno further discloses the step of generating a schedule of machine instructions in accordance with said graph representation, wherein said machine instructions in said schedule of machine instructions corresponding to said second operation are scheduled after said machine instructions corresponding to said first operation (see Fig. 1, which shows generating a schedule of instructions; see also column 10, lines 50-60, which shows ensuring that instructions are executed in the order prescribed by the dependencies).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Moreno with the features taught by Bharadwaj, for the purpose of determining whether reordering memory operations affects the meaning of the source code (see Bharadwaj, column 6, lines 40-43).

With respect to claim 13, see the explanation for claim 1 above. Note that Moreno shows a computer program product for use in a computer system (see column 1, lines 18-22).

With respect to claim 14, see the explanation for claim 2 above.

With respect to claim 17, see the explanation for claim 5 above.

With respect to claim 19, see the explanation for claim 7 above.

With respect to claim 20, see the explanation for claim 8 above.

Art Unit: 2122

With respect to claim 21, see the explanation for claim 9 above.

With respect to claim 22, see the explanation for claim 10 above.

With respect to claim 23, see the explanation for claim 11 above.

With respect to claim 24, see the explanation for claim 12 above.

With respect to claim 25, see the explanation for claim 1 above. Note that Moreno shows a computer system comprising a memory and a processor (see Figs. 3 and 5).

With respect to claim 26, see the explanation for claim 2 above.

With respect to claim 29, see the explanation for claim 5 above.

With respect to claim 31, see the explanation for claim 7 above.

With respect to claim 32, see the explanation for claim 8 above.

With respect to claim 33, see the explanation for claim 9 above.

With respect to claim 34, see the explanation for claim 10 above.

With respect to claim 35, see the explanation for claim 11 above.

With respect to claim 36, see the explanation for claim 12 above.

5. Claims 3, 4, 15, 16, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno in view of Bharadwaj as applied to claims 1, 2, 5, 7-14, 17, 19-26, 29, and 31-36 above, and further in view of U.S. Pat. No. 6,016,398 to Radigan (hereinafter Radigan 398).

With respect to claim 3, Moreno in view of Bharadwaj does not expressly disclose the limitation wherein said graph representation is an intermediate representation.

Radigan 398 discloses the limitation above in a system for removing dependencies (see Fig. 2A, which shows creating an intermediate representation of a program comprising nodes for

Art Unit: 2122

a graph), in order to ensure that each variable expression will be reached by at most one definition (see column 6, lines 56-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Moreno and Bharadwaj with the features taught by Radigan 398, for the purpose of ensuring the consistency of variable definitions.

With respect to claim 4, Moreno in view of Bharadwaj does not expressly disclose the limitation wherein said intermediate representation is a single static assignment graph embedded in a control flow graph.

Radigan 398 further discloses the limitation above (see Fig. 4A, which shows determining the flow of control along each execution path; see also Fig. 3A and column 14, lines 14-16, which shows a corresponding graph; see also column 6, lines 56-61, which shows using static single assignment, or SSA, in order to ensure that each variable expression will be reached by at most one definition).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Moreno and Bharadwaj with the features taught by Radigan 398, for the purpose of ensuring the consistency of variable definitions.

With respect to claim 15, see the explanation for claim 3 above.

With respect to claim 16, see the explanation for claim 4 above.

With respect to claim 27, see the explanation for claim 3 above.

With respect to claim 28, see the explanation for claim 4 above.

Art Unit: 2122

6. Claims 6, 18 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno in view of Bharadwaj as applied to claims 1, 2, 5, 7-14, 17, 19-26, 29, and 31-36 above, and further in view of U.S. Pat. No. 6,151,704 to Radigan (hereinafter Radigan 704).

Moreno in view of Bharadwaj does not expressly disclose the limitation wherein said first memory operation is positioned before a repetitive loop in said procedure and said second memory operation is within said repetitive loop; said graphic representation including a phi node that corresponds to a loop back position in said repetitive loop.

Radigan 704 discloses the limitation above for the purpose of optimizing a loop in a computer program (see column 6, lines 3-11, which shows a memory operation within a loop and a memory operation prior to the loop; see also column 4, lines 32-36, which shows the use of phi functions or phi nodes to denote a merge point, such as a loop back position).

Radigan 704 further discloses the limitations wherein:

(a) when a memory operation having the same location type as said first and second memory operation exists in said loop, said new position in said graph representation is a position that is serially dependent upon said phi node (see column 6, lines 3-11, which shows determining whether a memory operation writes to a variable referenced by the first and second memory operations, and thus has the same location type and is dependent upon the phi node); and

(b) when a memory operation having the same location type as said first and second memory operation does not exist in said loop, said new position in said graph representation is a position that is not serially dependent on any operation in the loop (see column 6, lines 3-11, which shows determining whether a memory operation is not within the loop and thus is not dependent upon instructions in the loop).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Moreno and Bharadwaj with the features taught by Radigan 704, for the purpose of optimizing loops in a computer program.

With respect to claim 18, see the explanation for claim 6 above.

With respect to claim 30, see the explanation for claim 6 above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Pat. No. 5,625,835 to Ebcioglu et al. discloses a method for reordering memory operations. U.S. Pat. No. 6,128,775 to Chow et al. discloses a method for optimizing the placement of load and store operations. U.S. Pat. No. 5,854,933 to Change discloses a method for moving loads and stores out of loops. U.S. Pat. No. 6,516,463 to Babaian et al. discloses a method for removing a dependency between a store and a load.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (703) 305-0352. The examiner can normally be reached on Monday through Friday from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Application/Control Number: 09/757,764

Page 13

Art Unit: 2122

MY

Michael J. Yigdall
Examiner
Art Unit 2122

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November 20, 2003

John Chavis

JOHN CHAVIS
PATENT EXAMINER
ART UNIT 2124